

Fig. 1

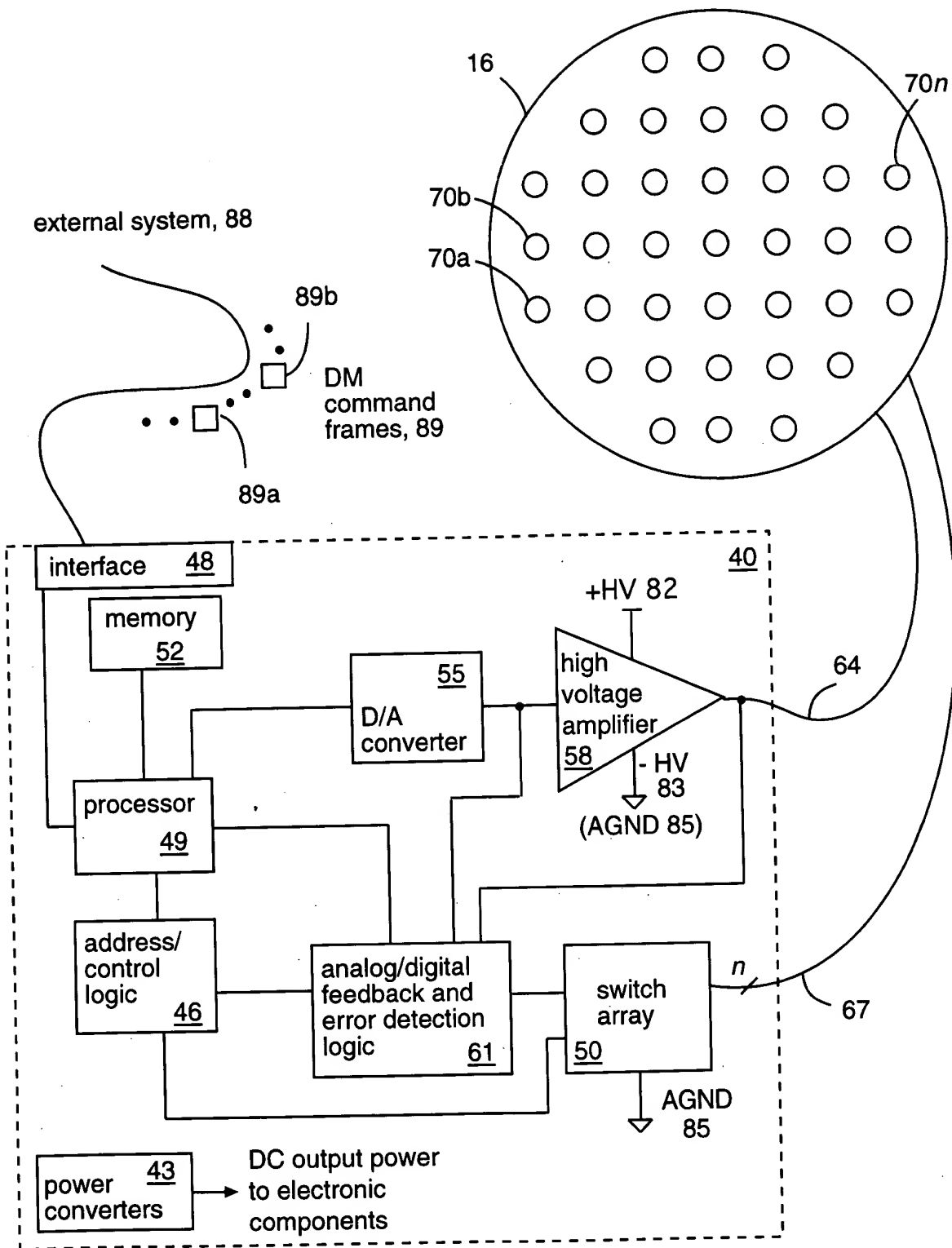


Fig. 2

The diagram illustrates a four-channel system (41a, 41b, 41c, 41d) connected to a central circular array (16). Each channel includes a D/A converter, processor, address/control logic, switch array, and high voltage amplifier. The central array has zones labeled A, B, C, D and is connected to a master processor (45) and an external system (88).

Channel 41a: Includes D/A converter A, processor A, address/control logic A, switch array A, and high voltage amplifier A. The switch array A is connected to the central array via line 64. The high voltage amplifier A is connected to the central array via line 50. The address/control logic A is connected to the central array via line 49. The processor A is connected to the central array via line 55. The D/A converter A is connected to the central array via line 67. The switch array A is also connected to ground (85).

Channel 41b: Includes D/A converter B, processor B, address/control logic B, switch array B, and high voltage amplifier B. The switch array B is connected to the central array via line 64. The high voltage amplifier B is connected to the central array via line 50. The address/control logic B is connected to the central array via line 49. The processor B is connected to the central array via line 55. The D/A converter B is connected to the central array via line 67. The switch array B is also connected to ground (85).

Channel 41c: Includes D/A converter C, processor C, address/control logic C, switch array C, and high voltage amplifier C. The switch array C is connected to the central array via line 64. The high voltage amplifier C is connected to the central array via line 50. The address/control logic C is connected to the central array via line 49. The processor C is connected to the central array via line 55. The D/A converter C is connected to the central array via line 67. The switch array C is also connected to ground (85).

Channel 41d: Includes D/A converter D, processor D, address/control logic D, switch array D, and high voltage amplifier D. The switch array D is connected to the central array via line 64. The high voltage amplifier D is connected to the central array via line 50. The address/control logic D is connected to the central array via line 49. The processor D is connected to the central array via line 55. The D/A converter D is connected to the central array via line 67. The switch array D is also connected to ground (85).

Central Array (16): A circular array with zones labeled A, B, C, D. The zones are arranged in a 2x2 grid. The zones are labeled 70a, 70b, 70c, and 70n. The array is connected to a master processor (45) and an external system (88).

Master Processor (45): Connected to the central array and the external system (88).

External System (88): Connected to the master processor (45).

Fig. 3

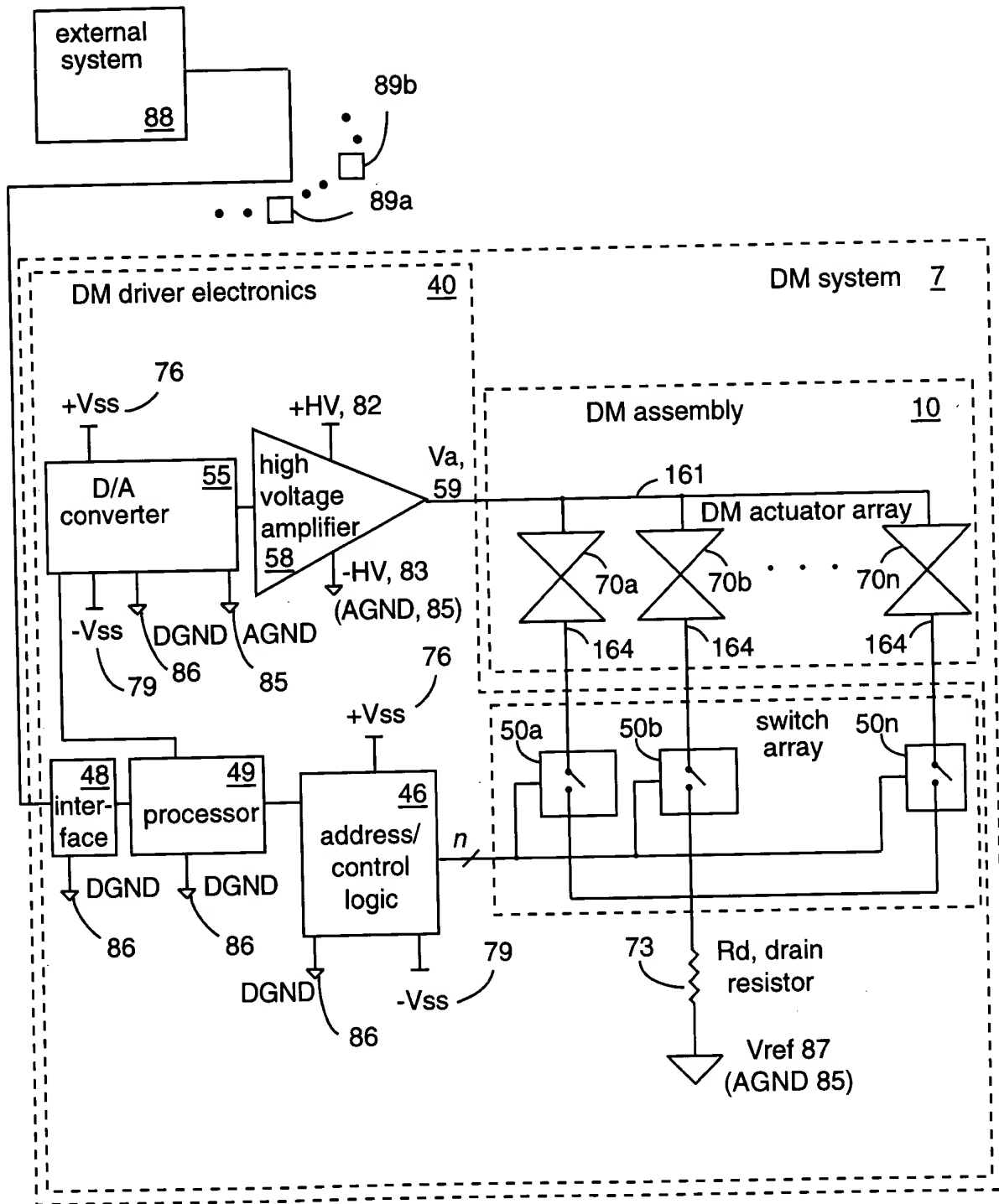


Fig. 4

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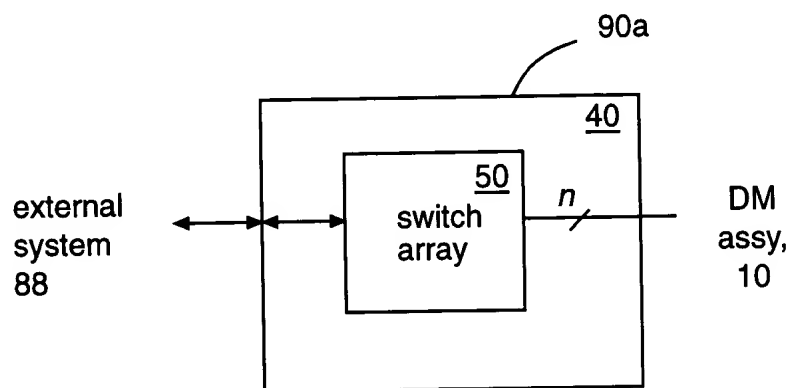


Fig. 5A

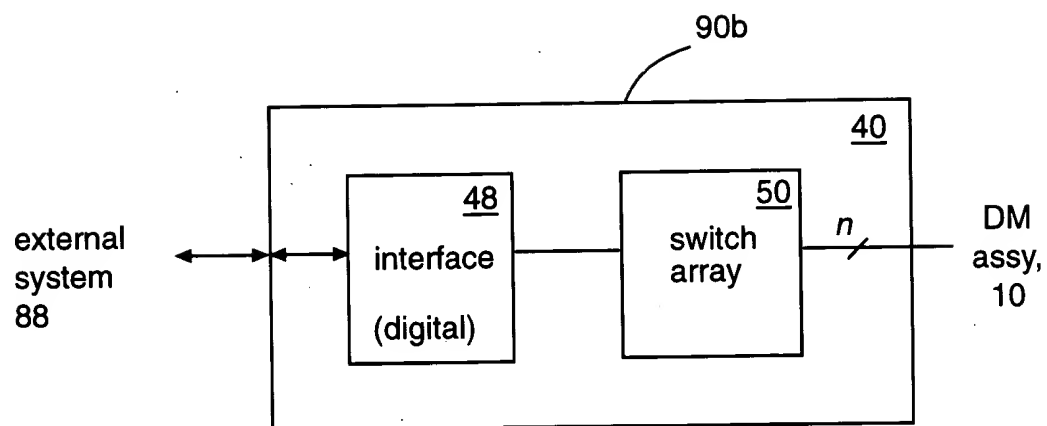


Fig. 5B

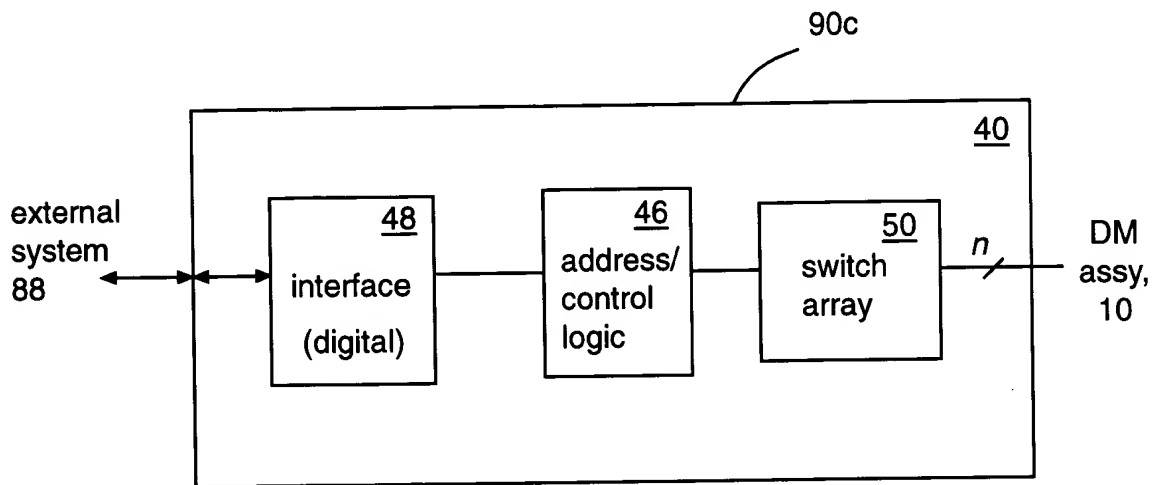


Fig. 5C

Variable	Mean	Standard Deviation	Minimum	Maximum
Age	34.5	10.2	21	55
Gender	0.5	0.5	0	1
Marital Status	0.4	0.5	0	1
Education	12.5	1.5	9	16
Income	15.2	5.8	5	35
Health	0.8	0.4	0	1
Stress	0.6	0.5	0	1
Depression	0.3	0.5	0	1
Life Satisfaction	0.7	0.4	0	1
Work Satisfaction	0.5	0.5	0	1
Family Satisfaction	0.6	0.5	0	1
Community Satisfaction	0.4	0.5	0	1
Overall Satisfaction	0.5	0.5	0	1

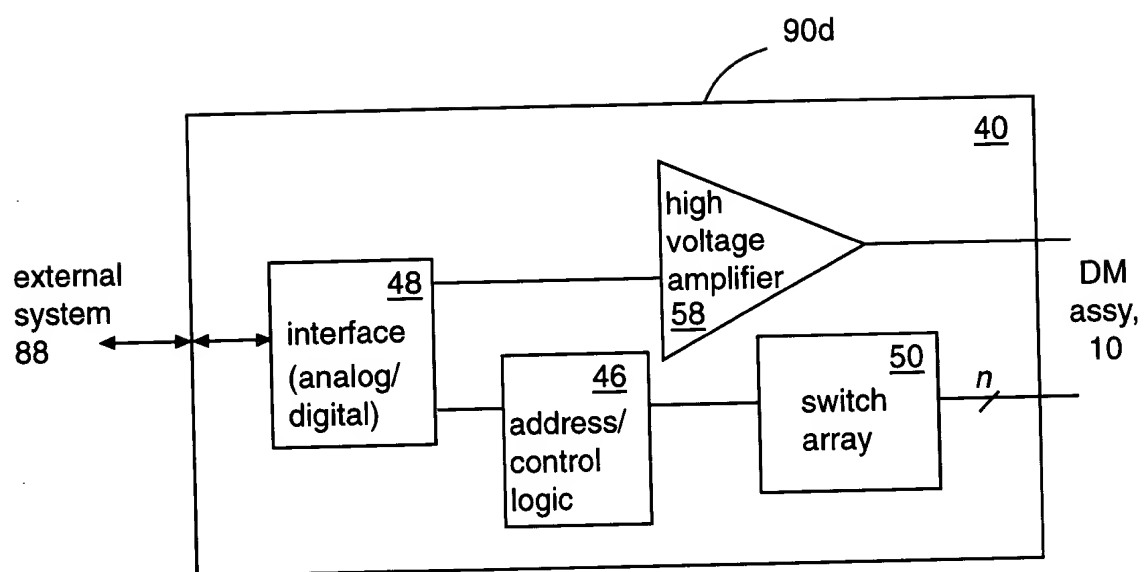


Fig. 5D

001120 30F300

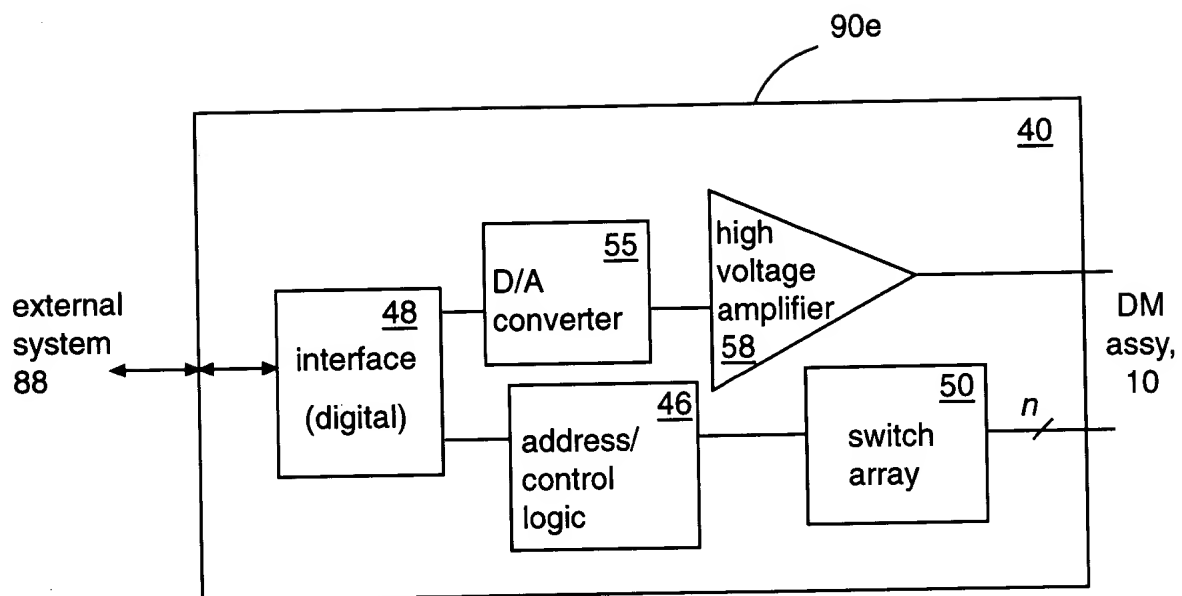


Fig. 5E

00000303300

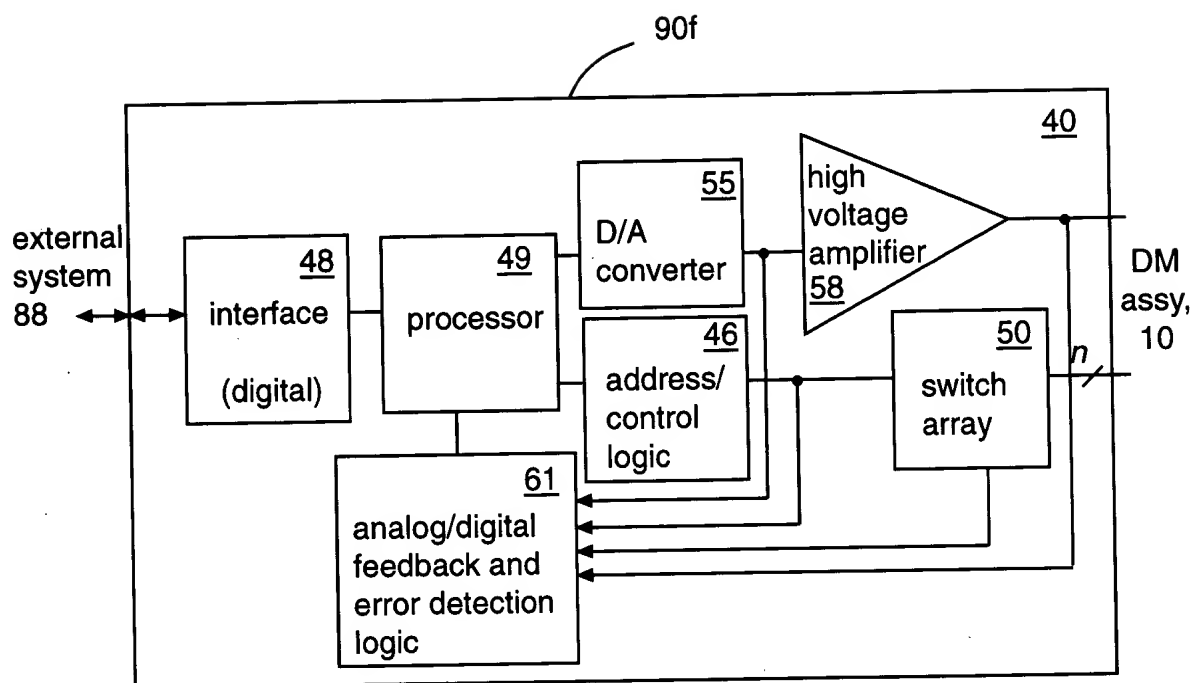


Fig. 5F

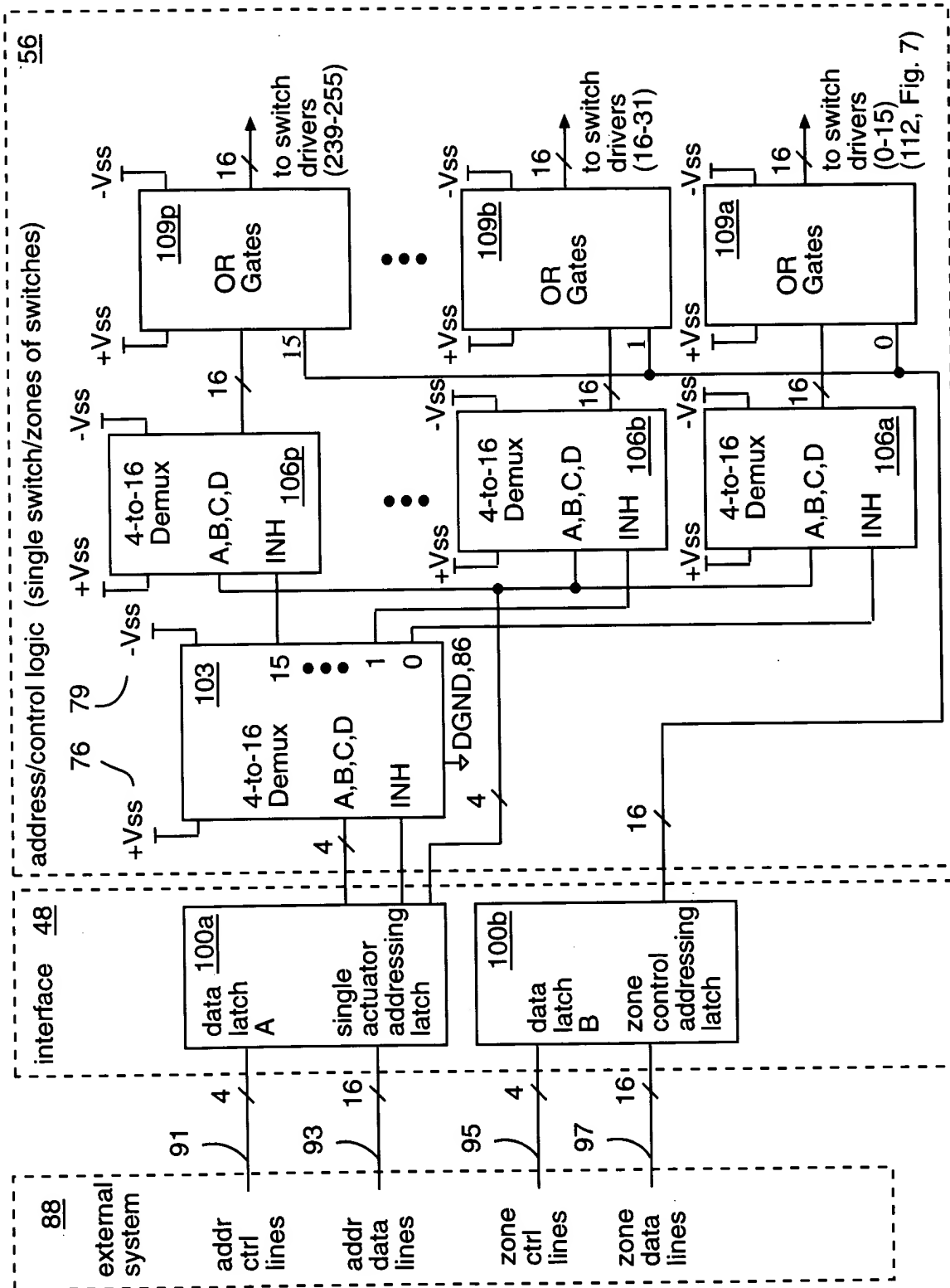


Fig. 6

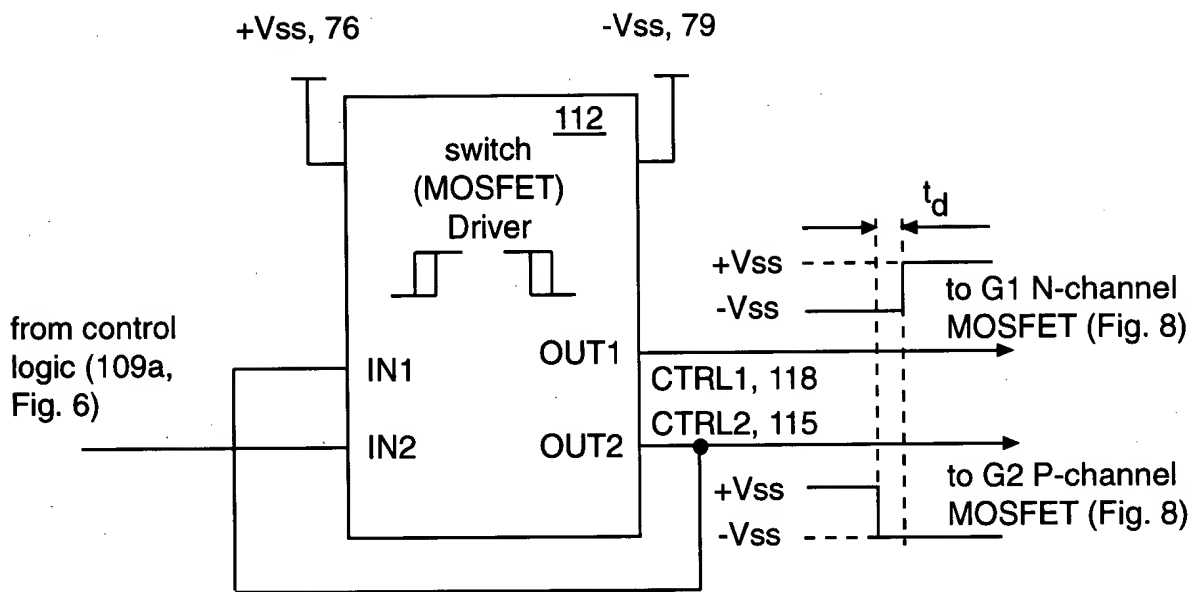


Fig. 7



Fig. 8

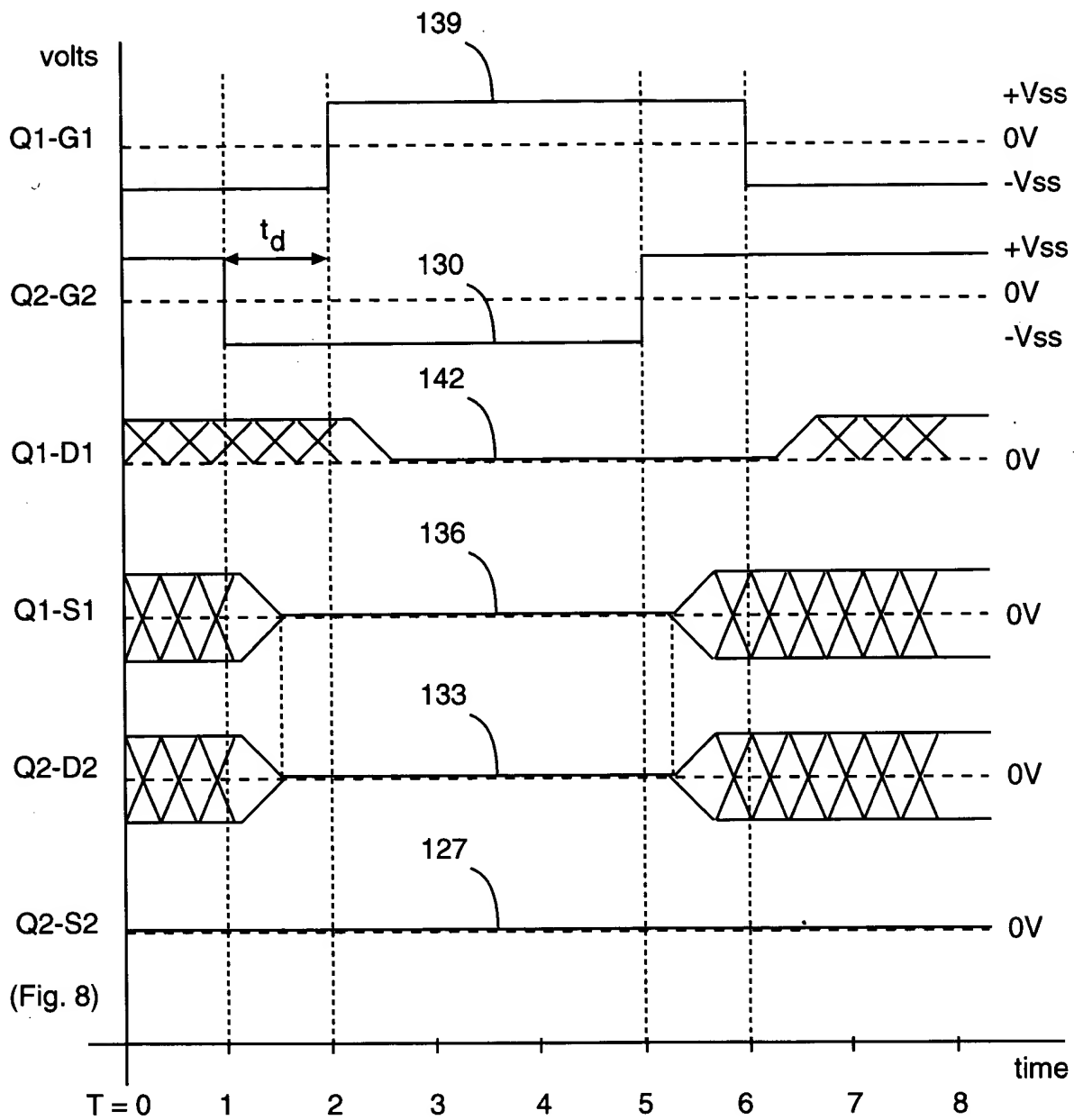


Fig. 9

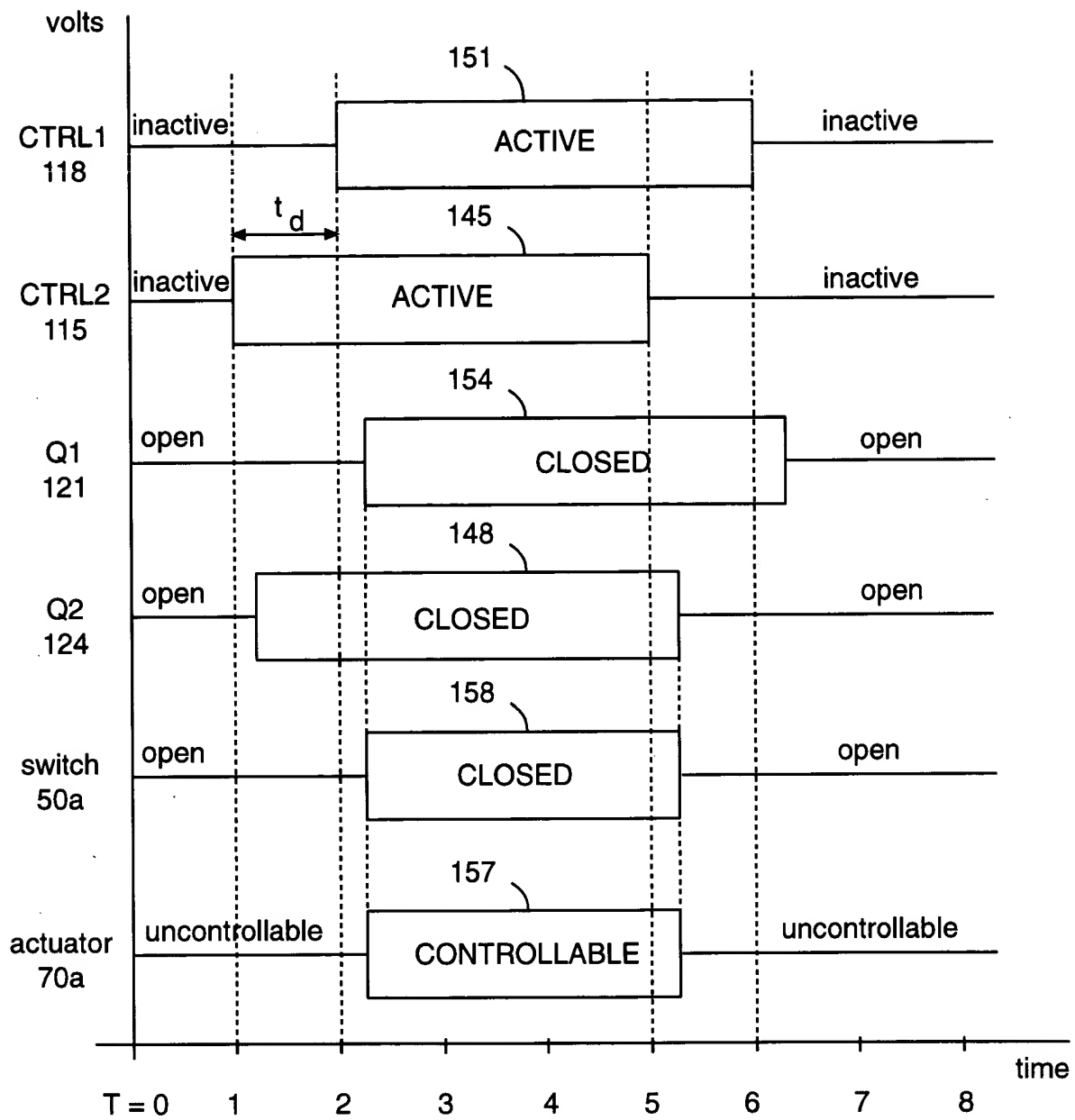


Fig. 10

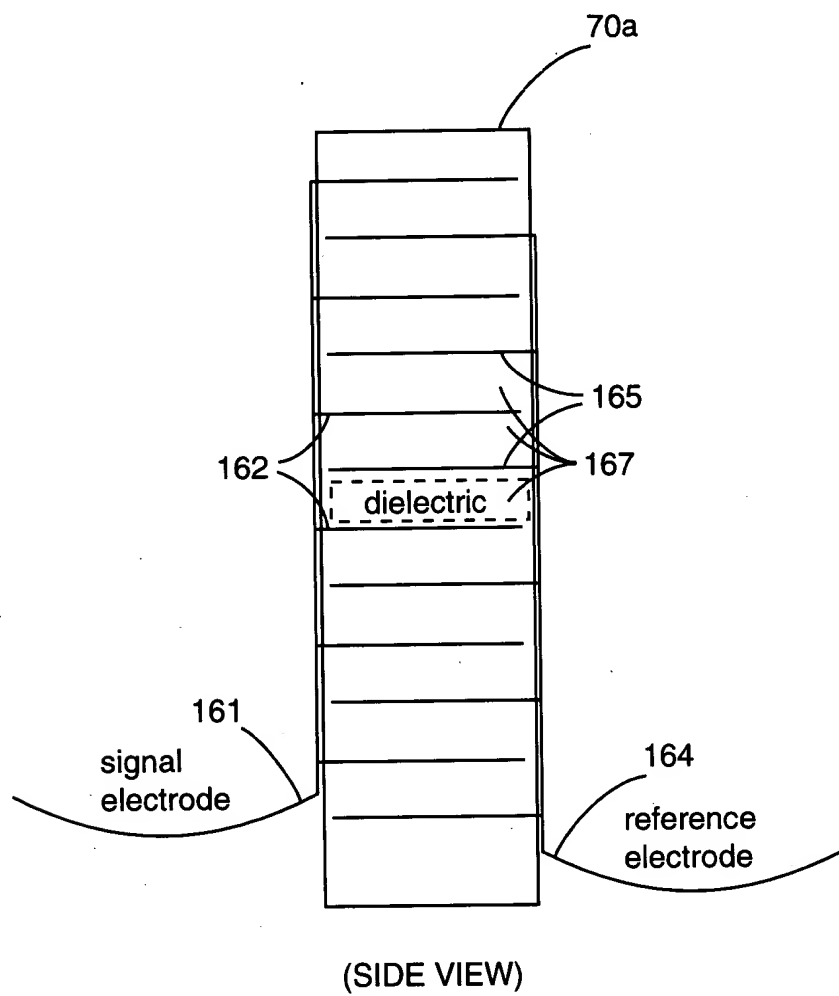


Fig. 11A

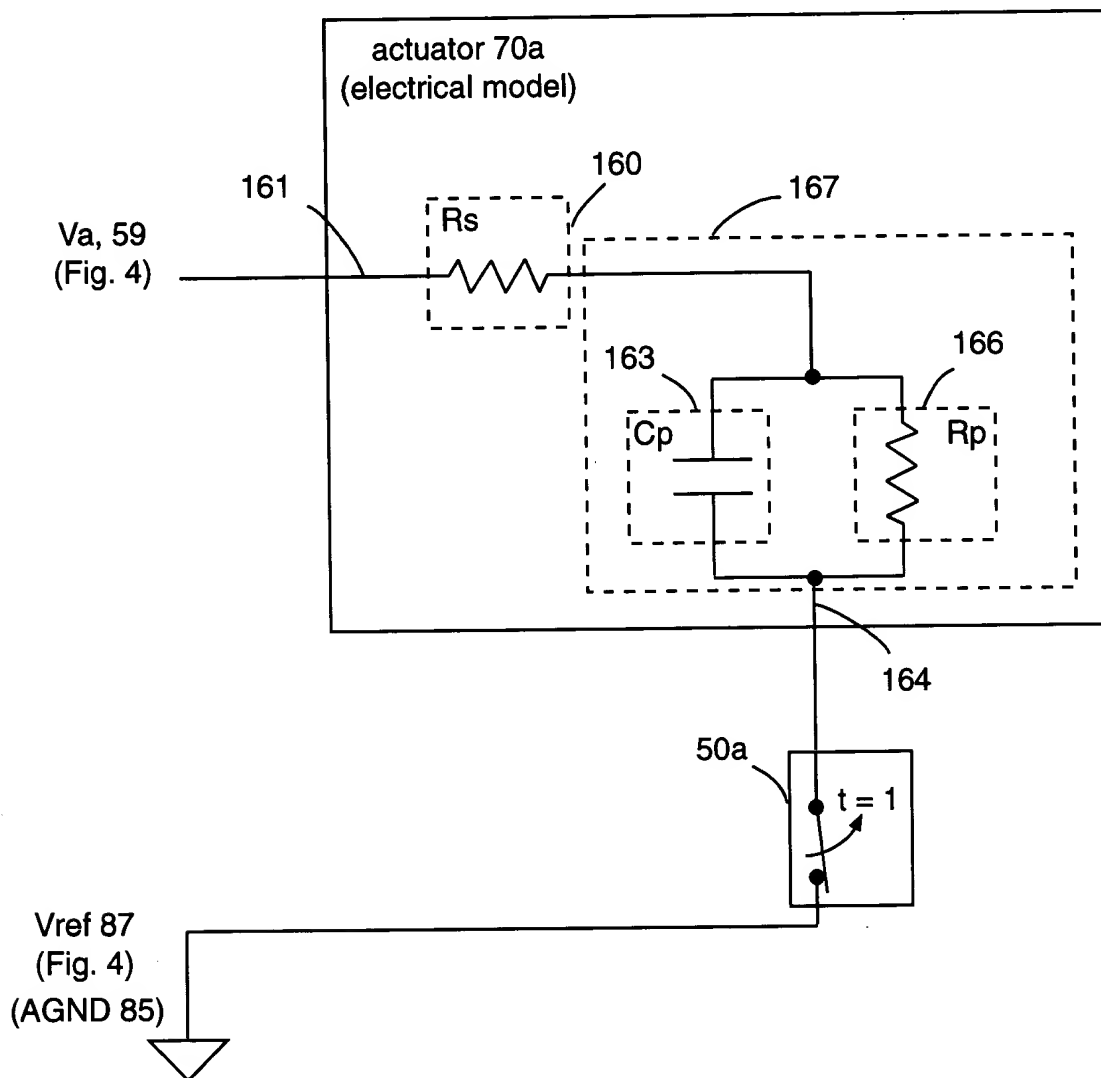


Fig. 11B

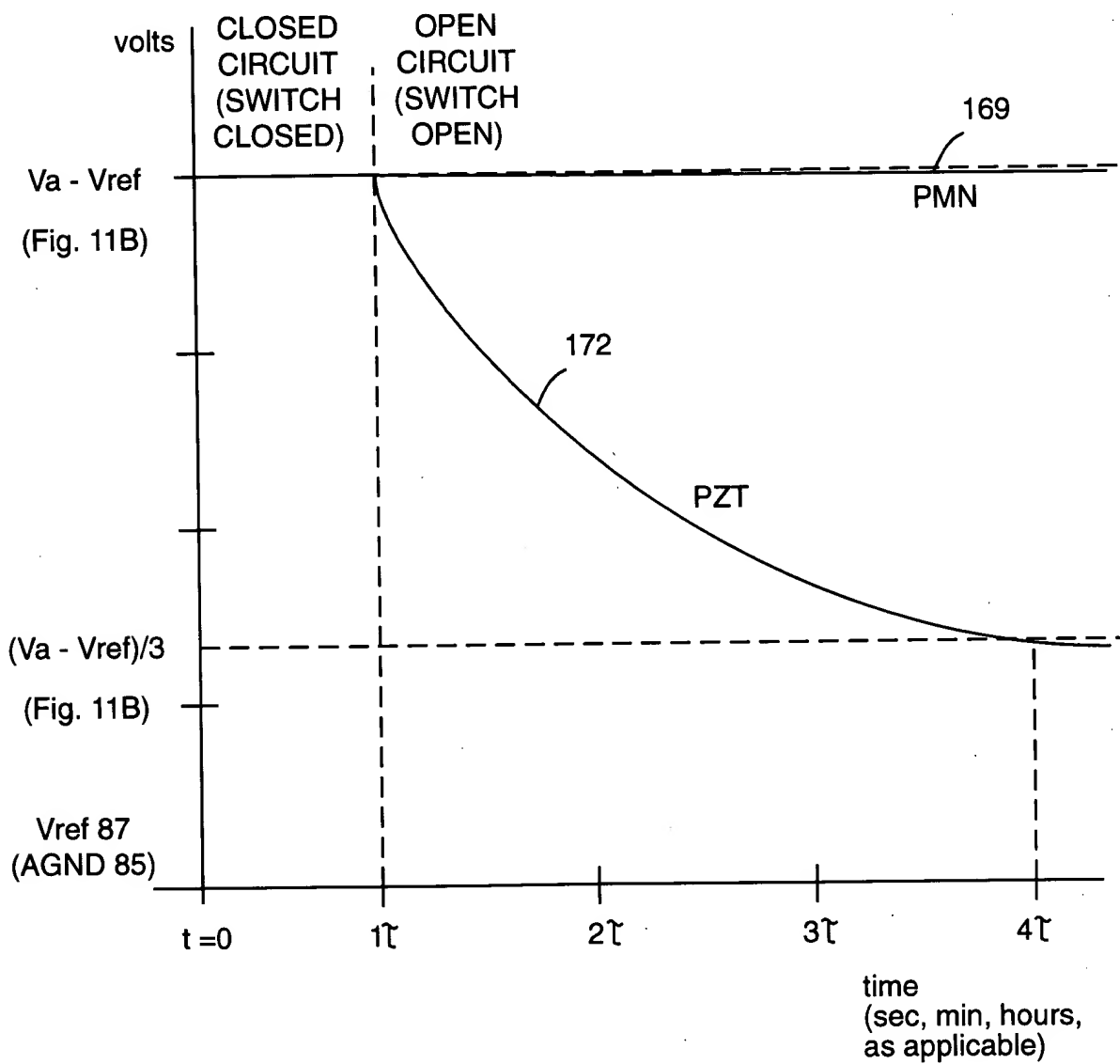


Fig. 12

[illegible]

Fig. 13

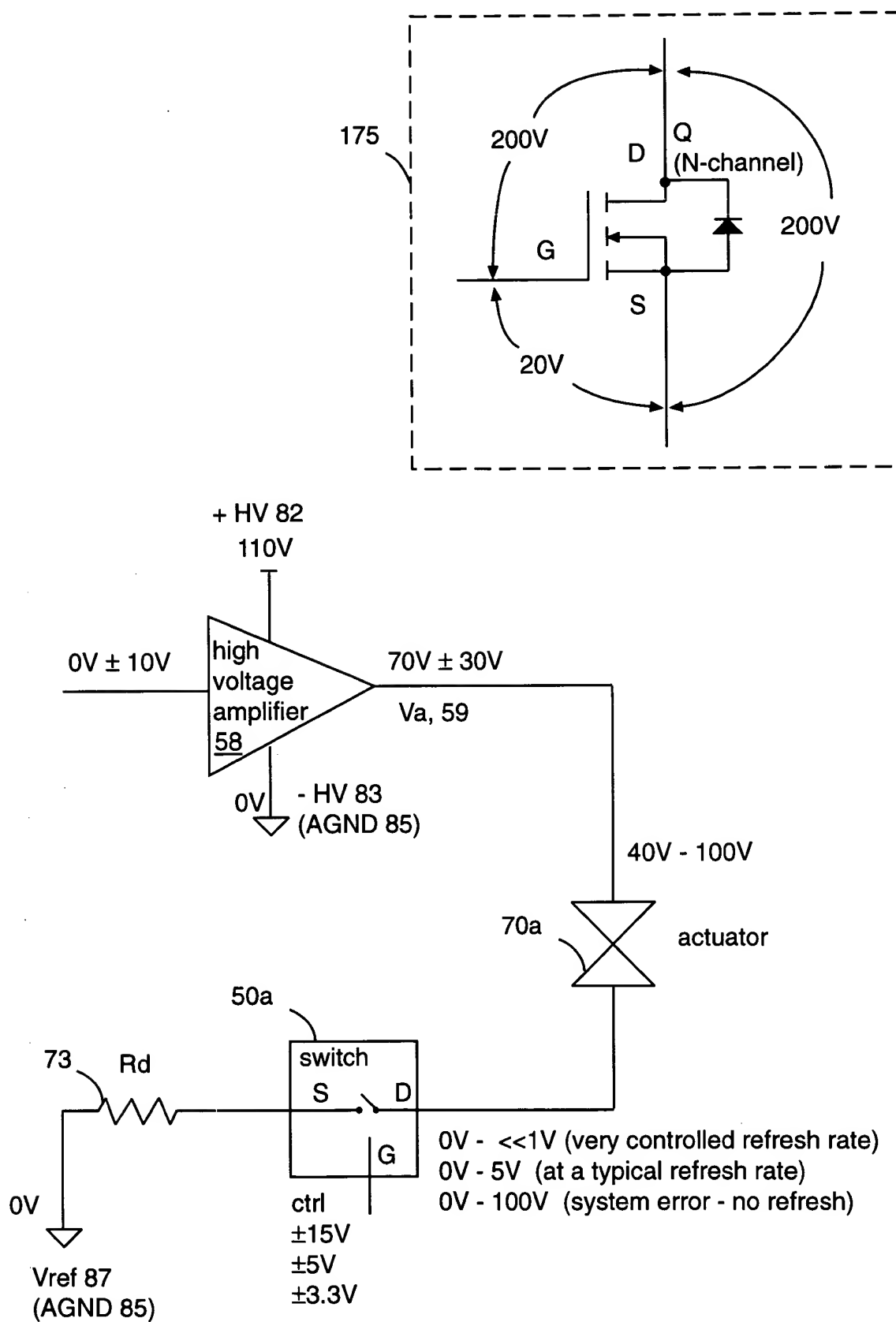
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Fig. 14

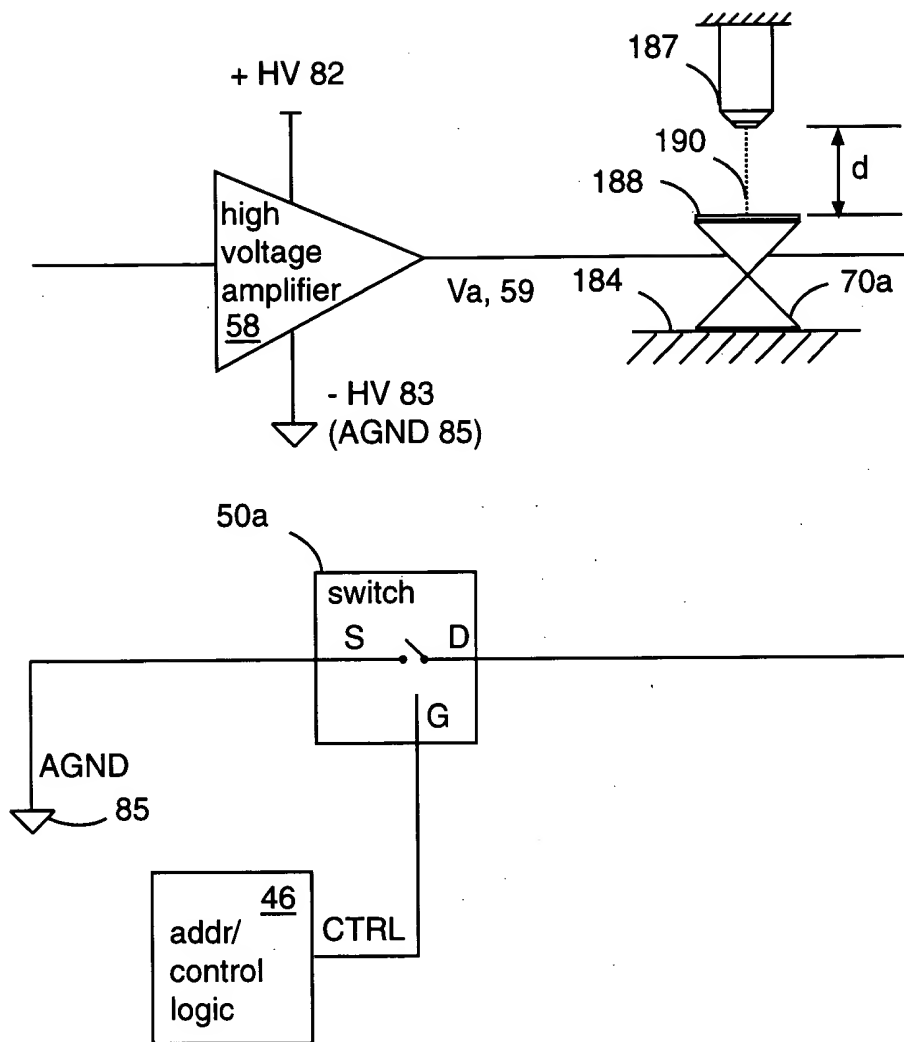


Fig. 15

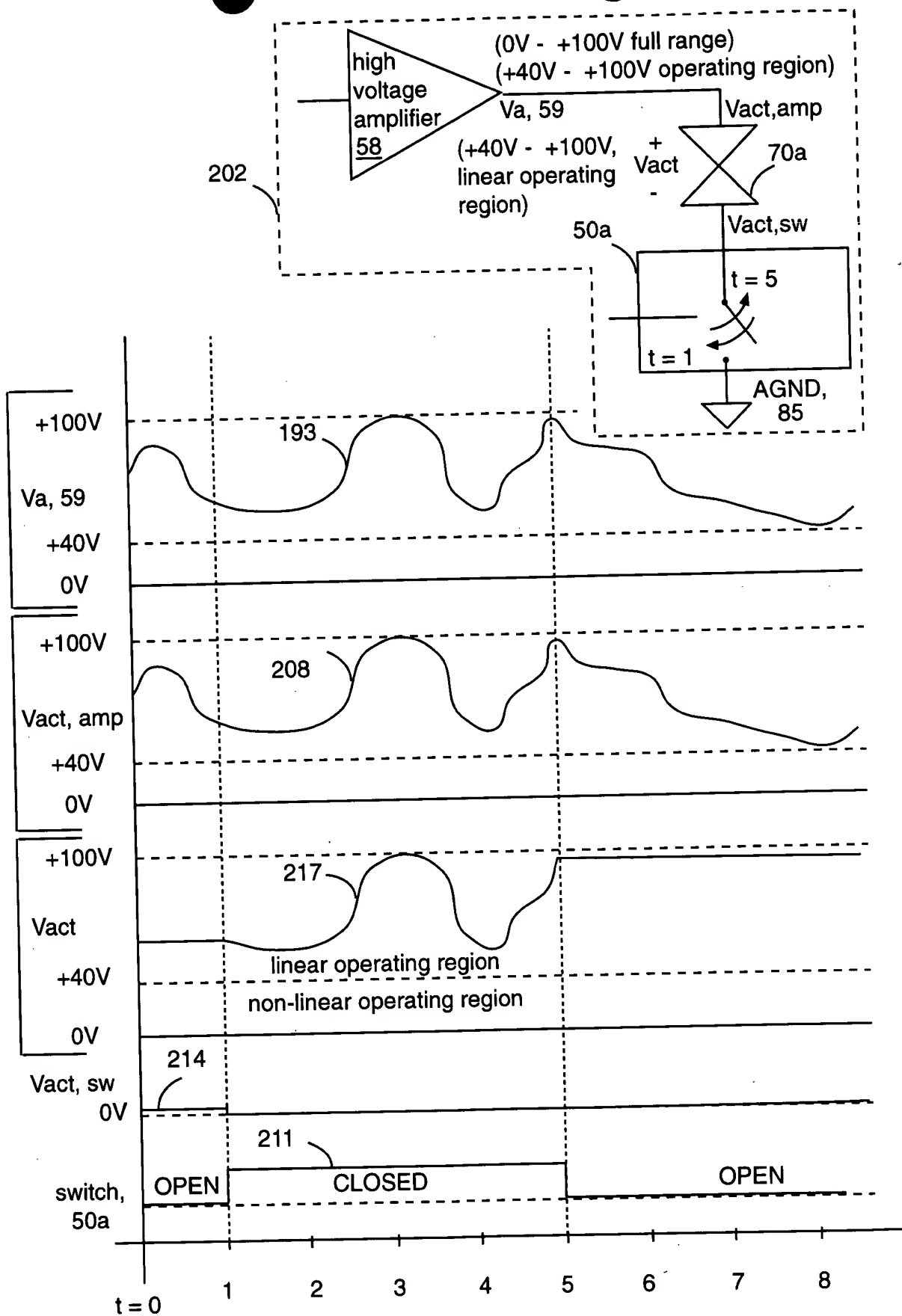


Fig. 17

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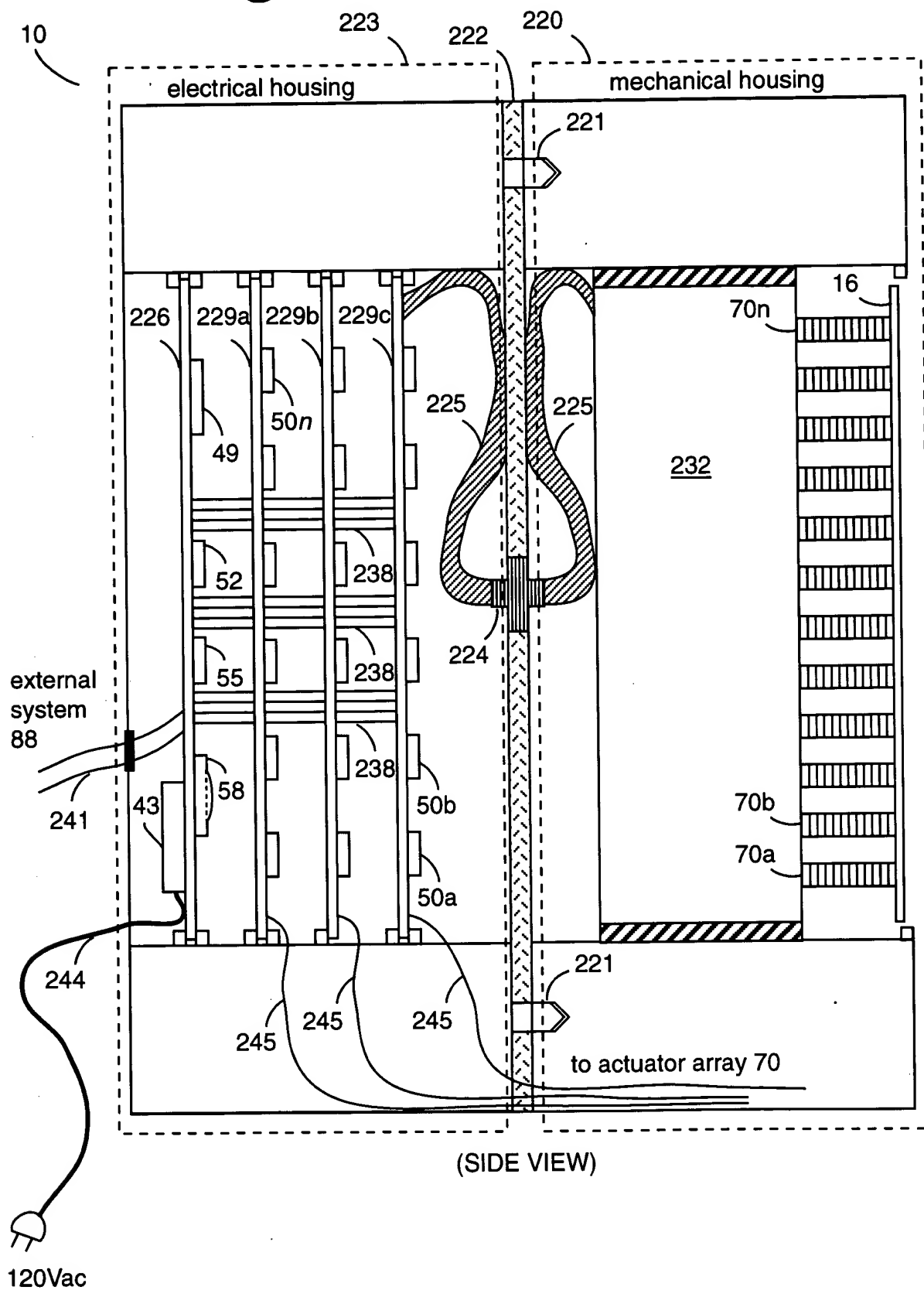


Fig. 18

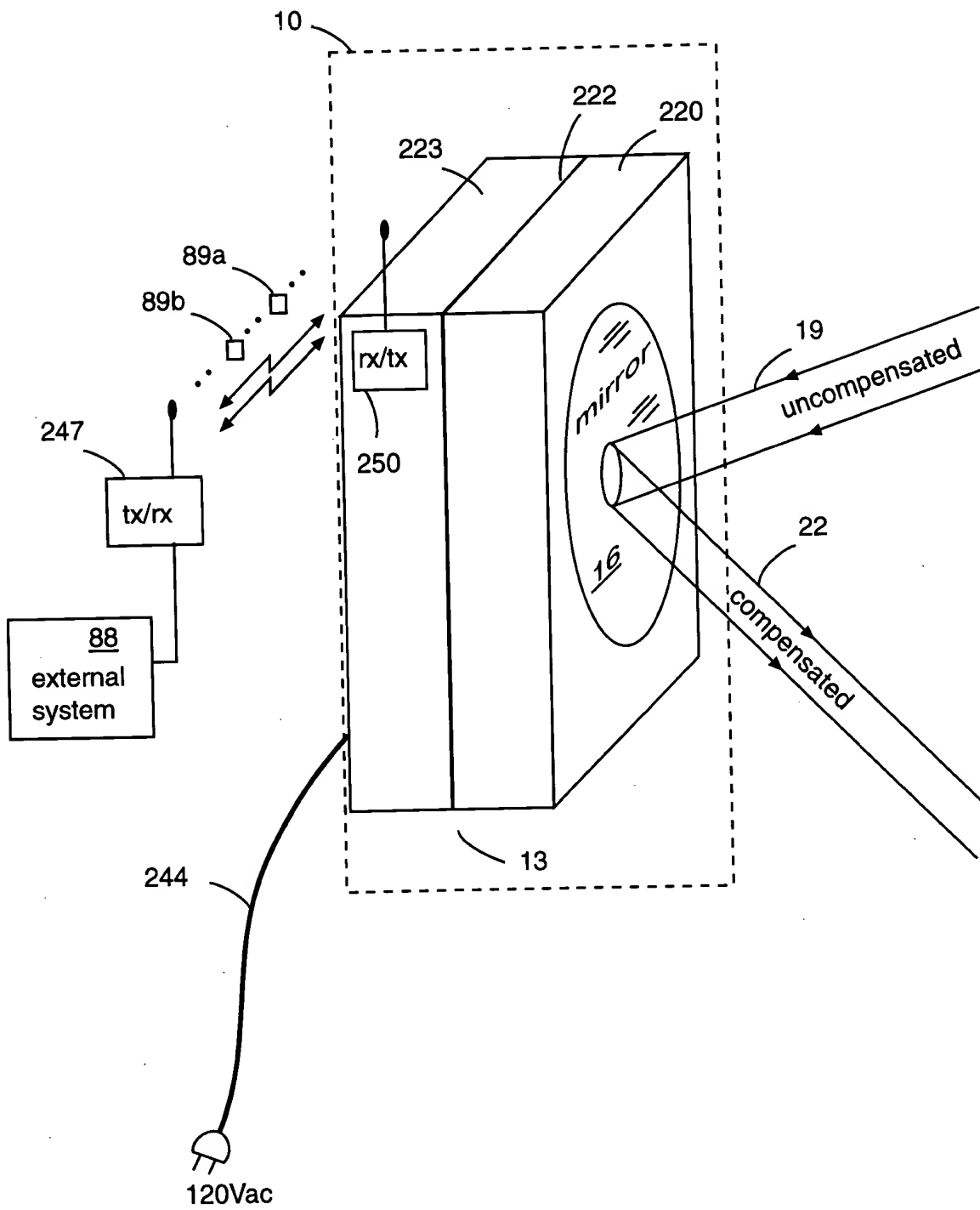


Fig. 19

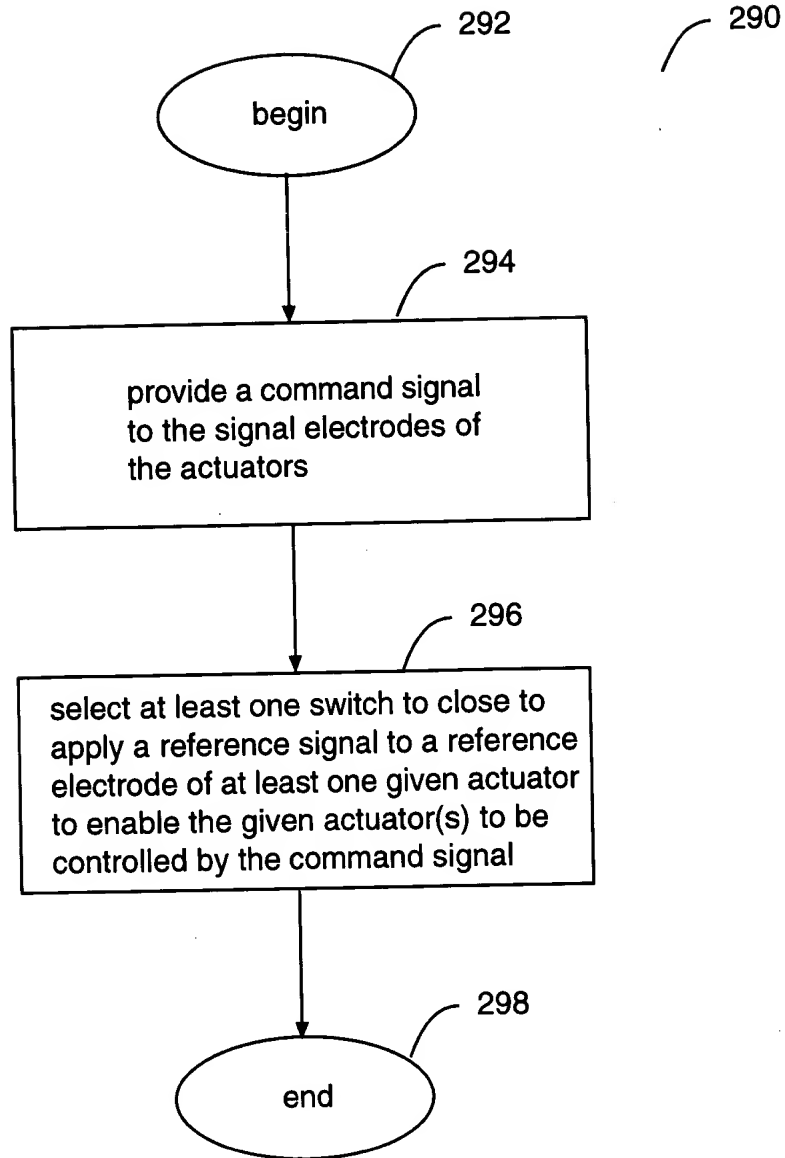
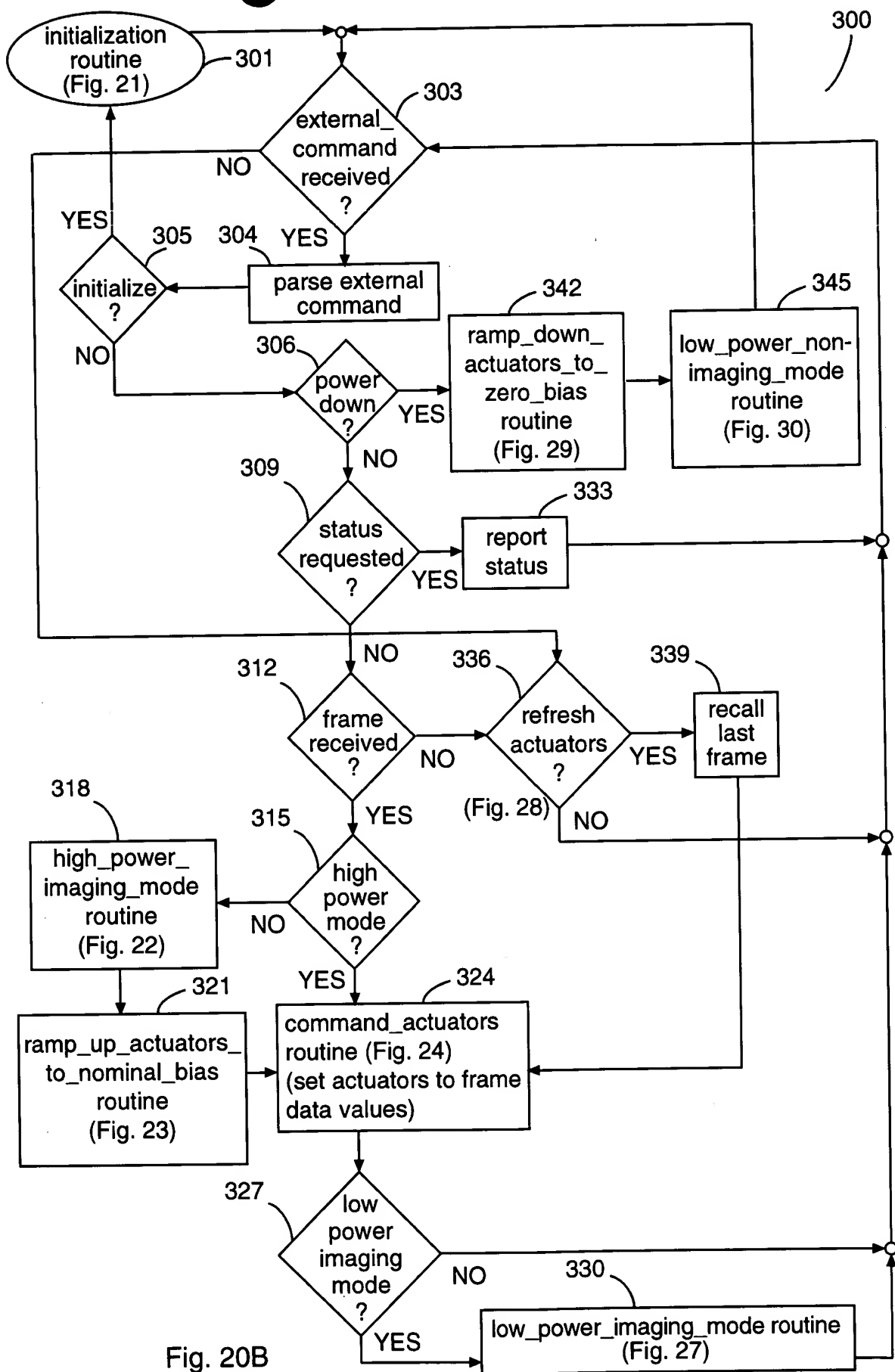


Fig. 20A



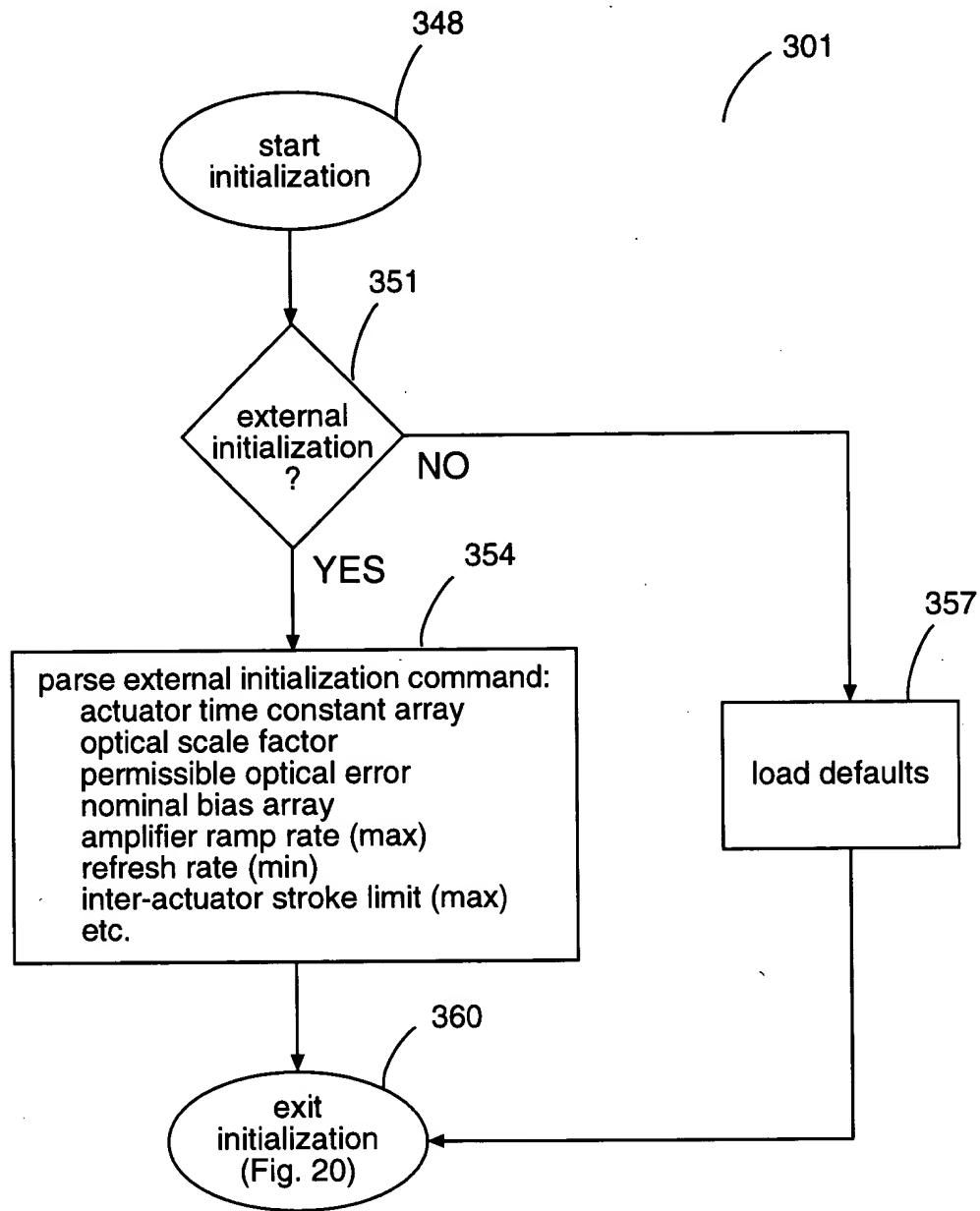


Fig. 21

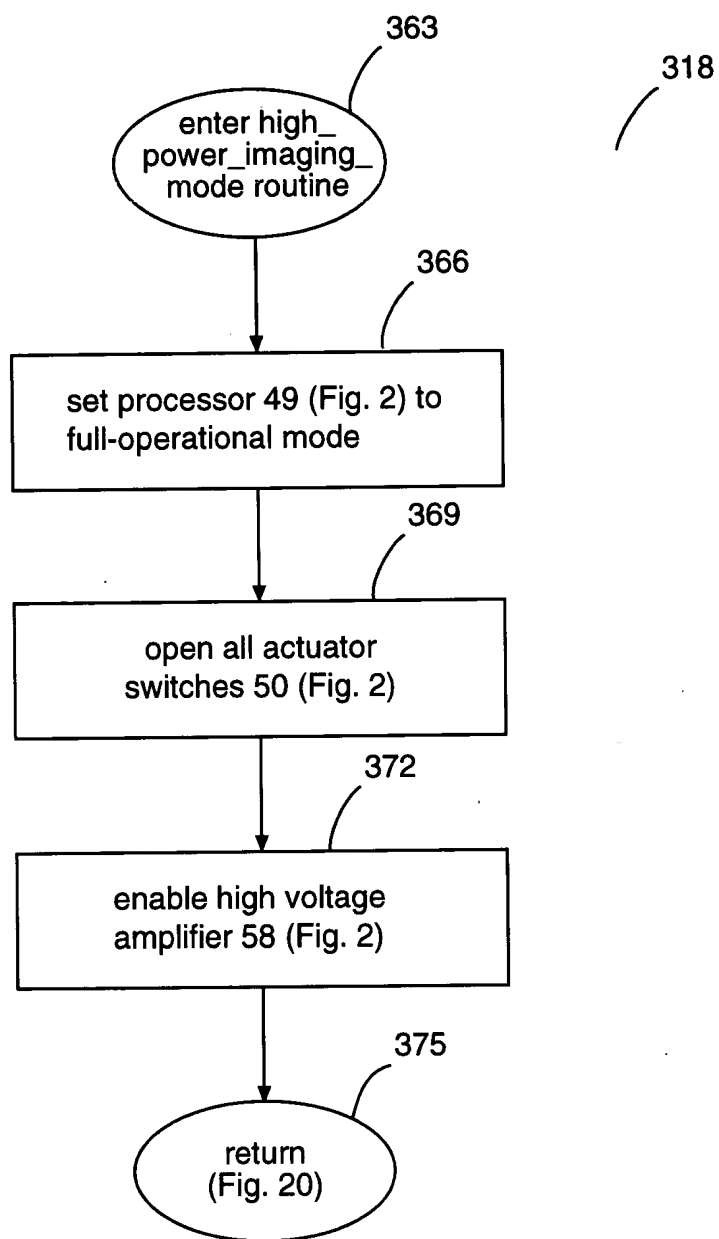


Fig. 22

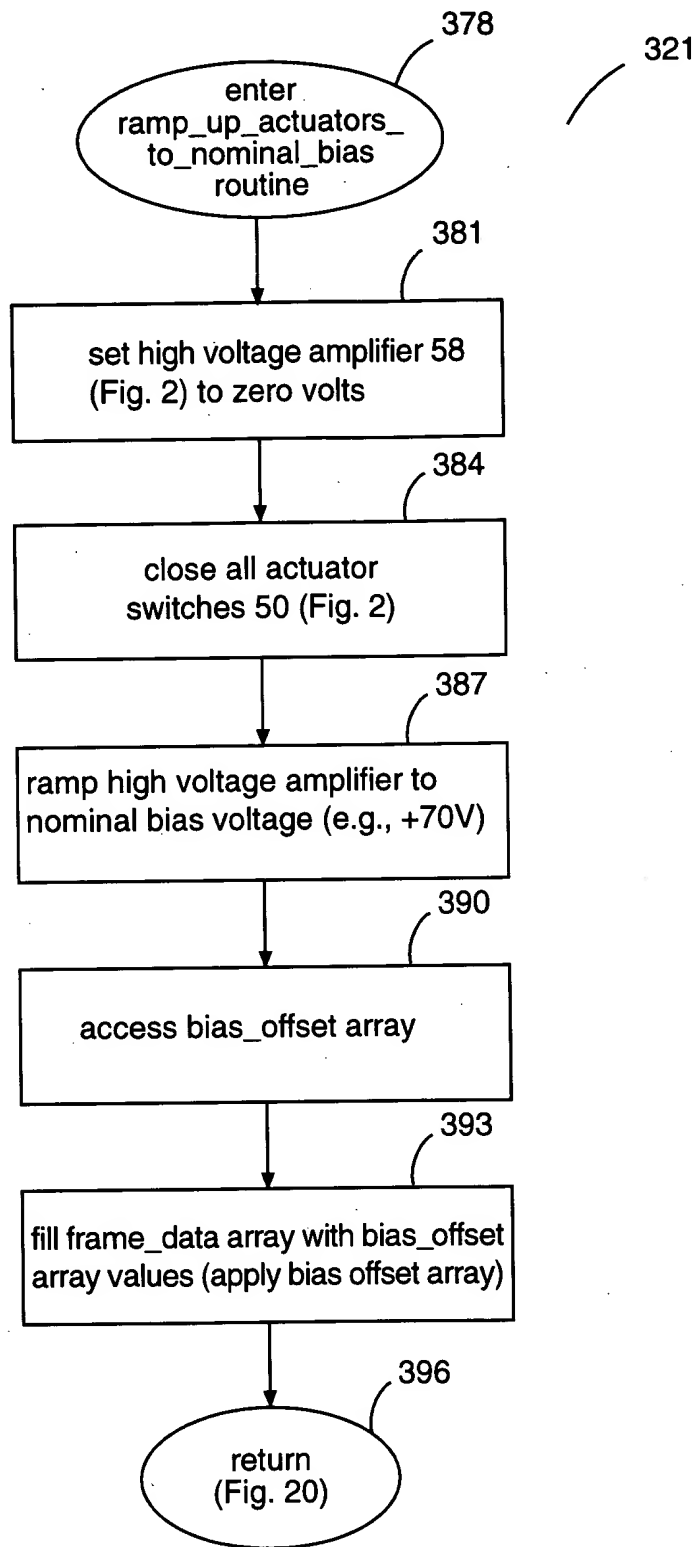


Fig. 23

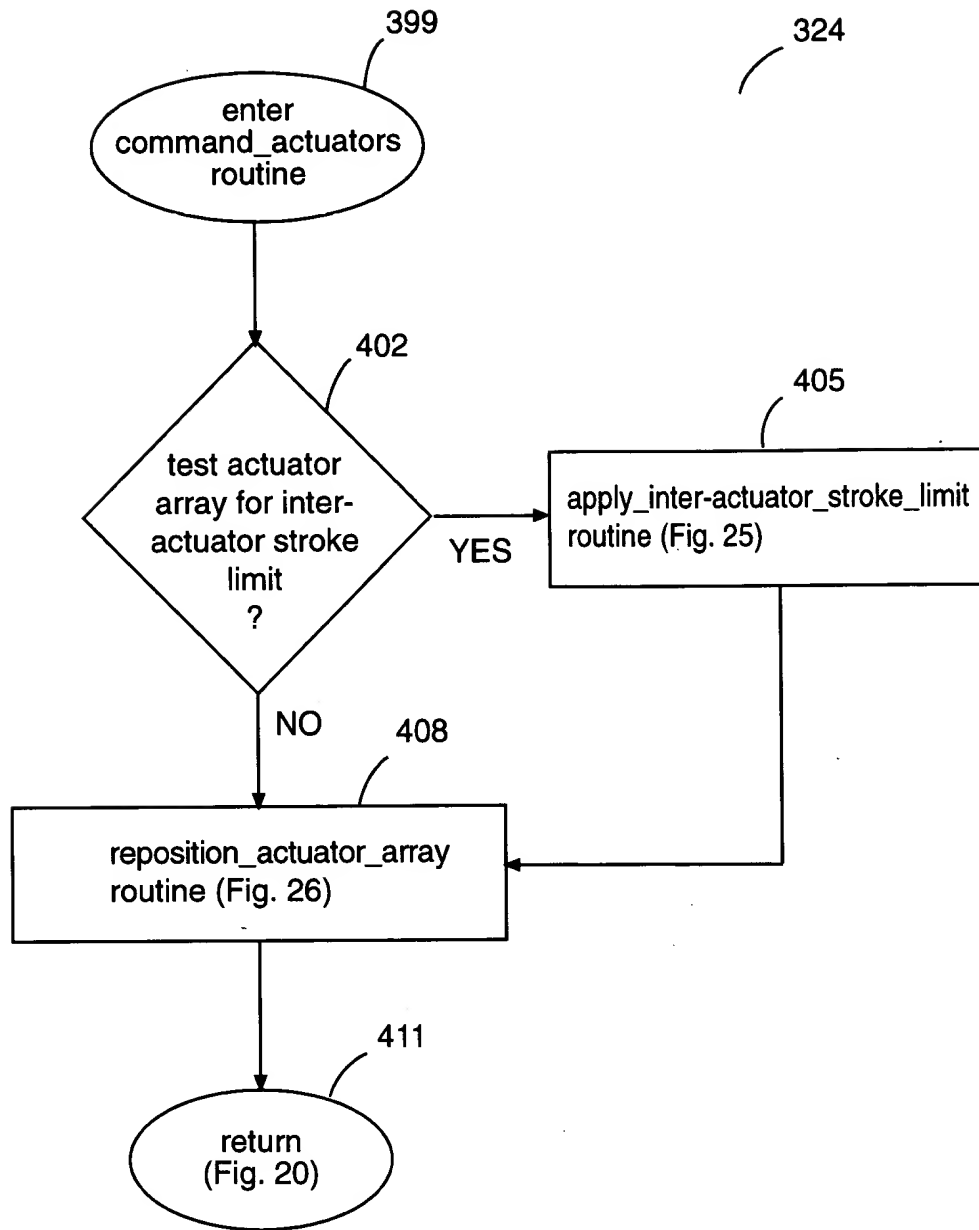


Fig. 24

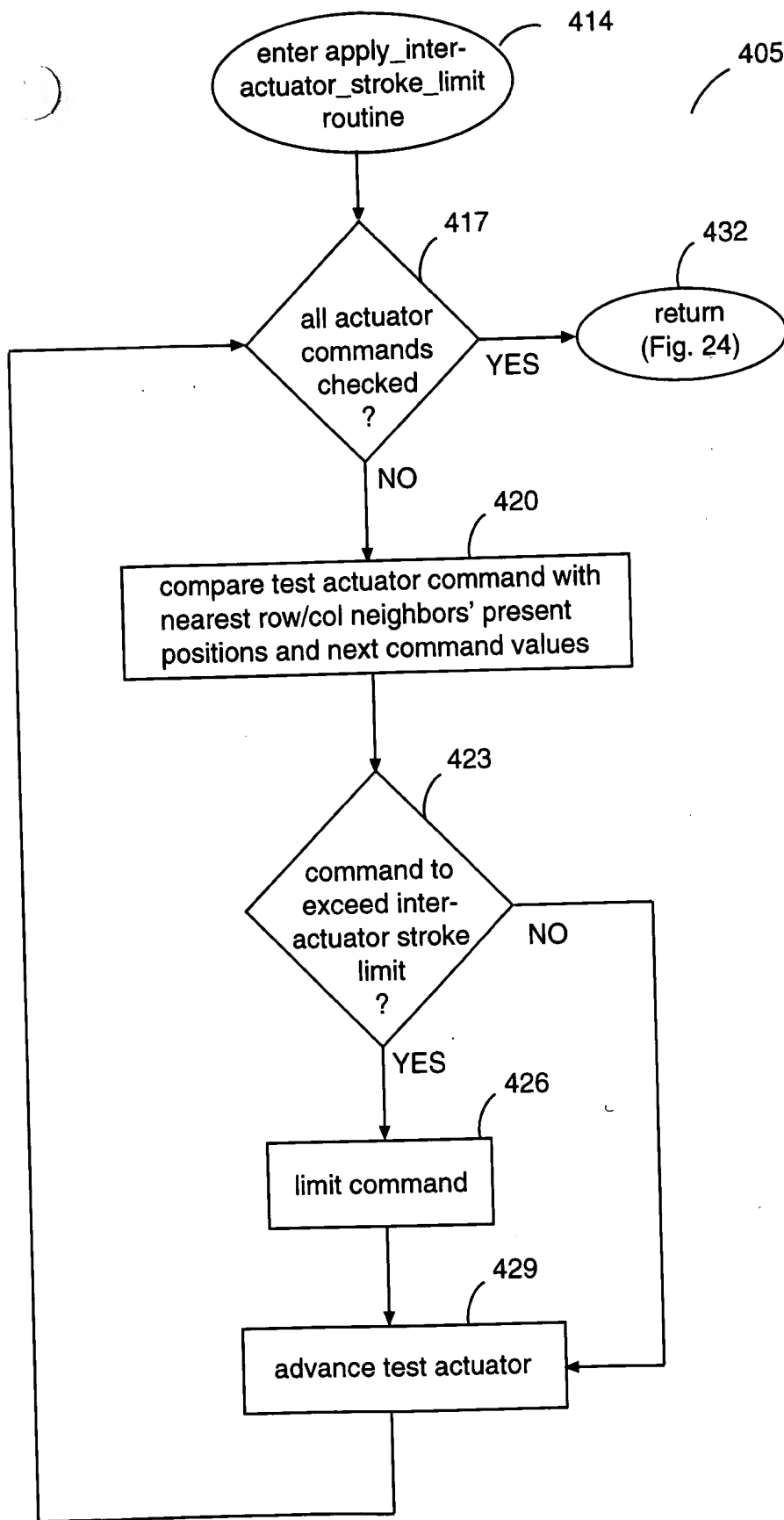


Fig. 25

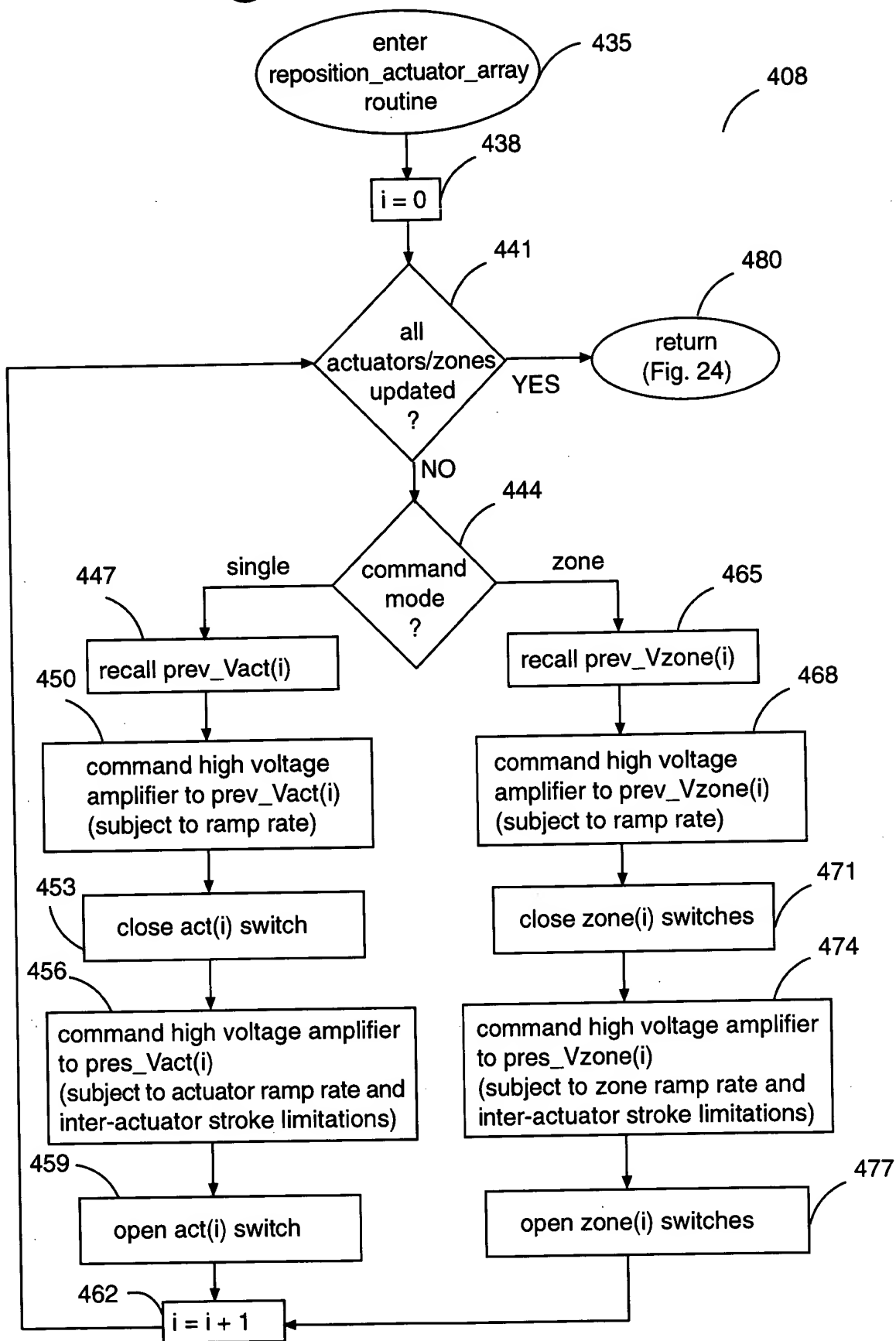


Fig. 26

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graph TD; 483([enter low_power_imaging_mode routine]) --> 486[disable high voltage amplifier]; 486 --> 488[enable refresh timer]; 488 --> 489[set refresh timer to min refresh rate]; 489 --> 492([return Fig. 20]);
```

330

483 enter low_power_imaging_mode routine

486 disable high voltage amplifier

488 enable refresh timer

489 set refresh timer to min refresh rate

492 return (Fig. 20)

Fig. 27

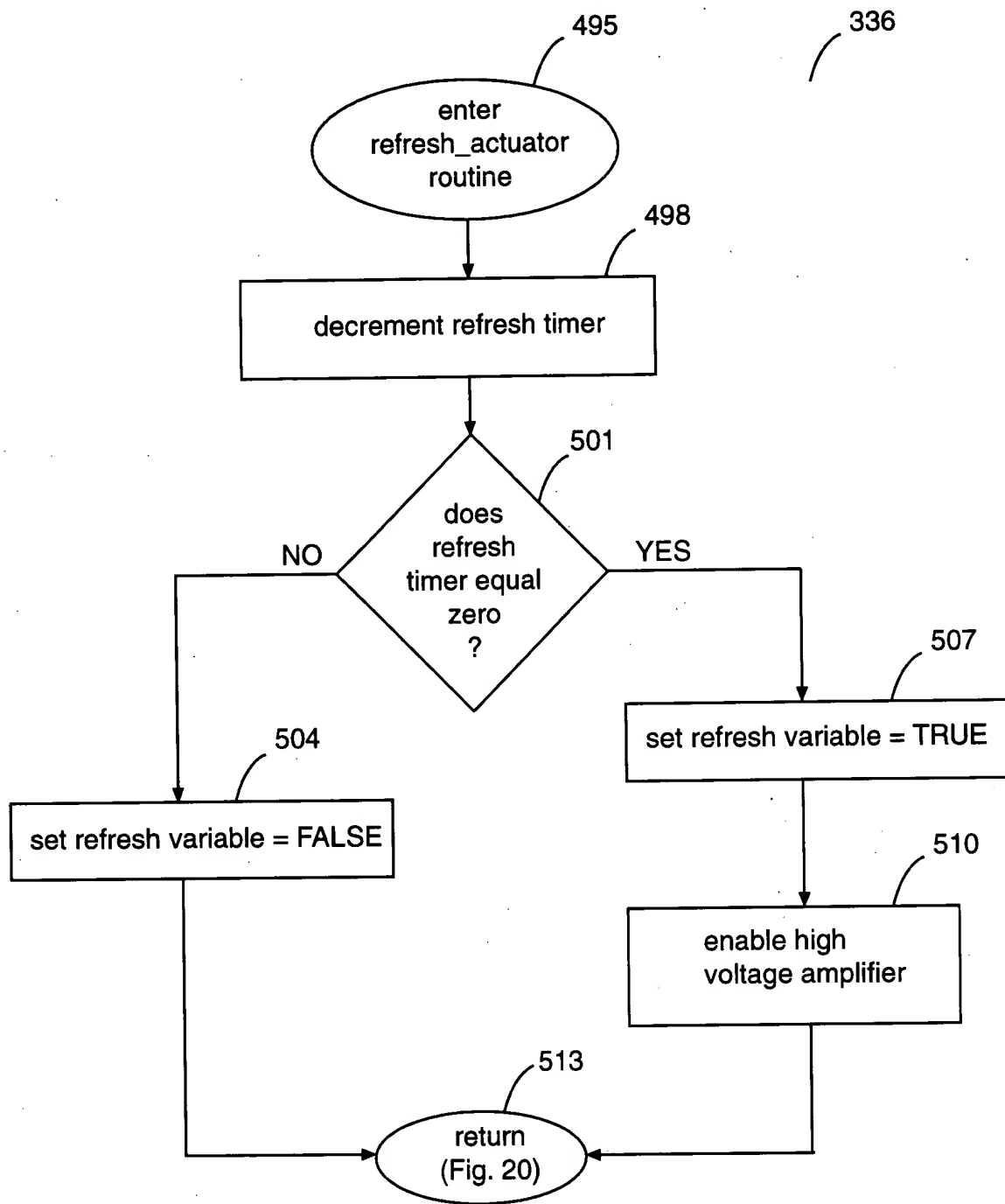


Fig. 28

U.S. Pat. No. 6,000,000

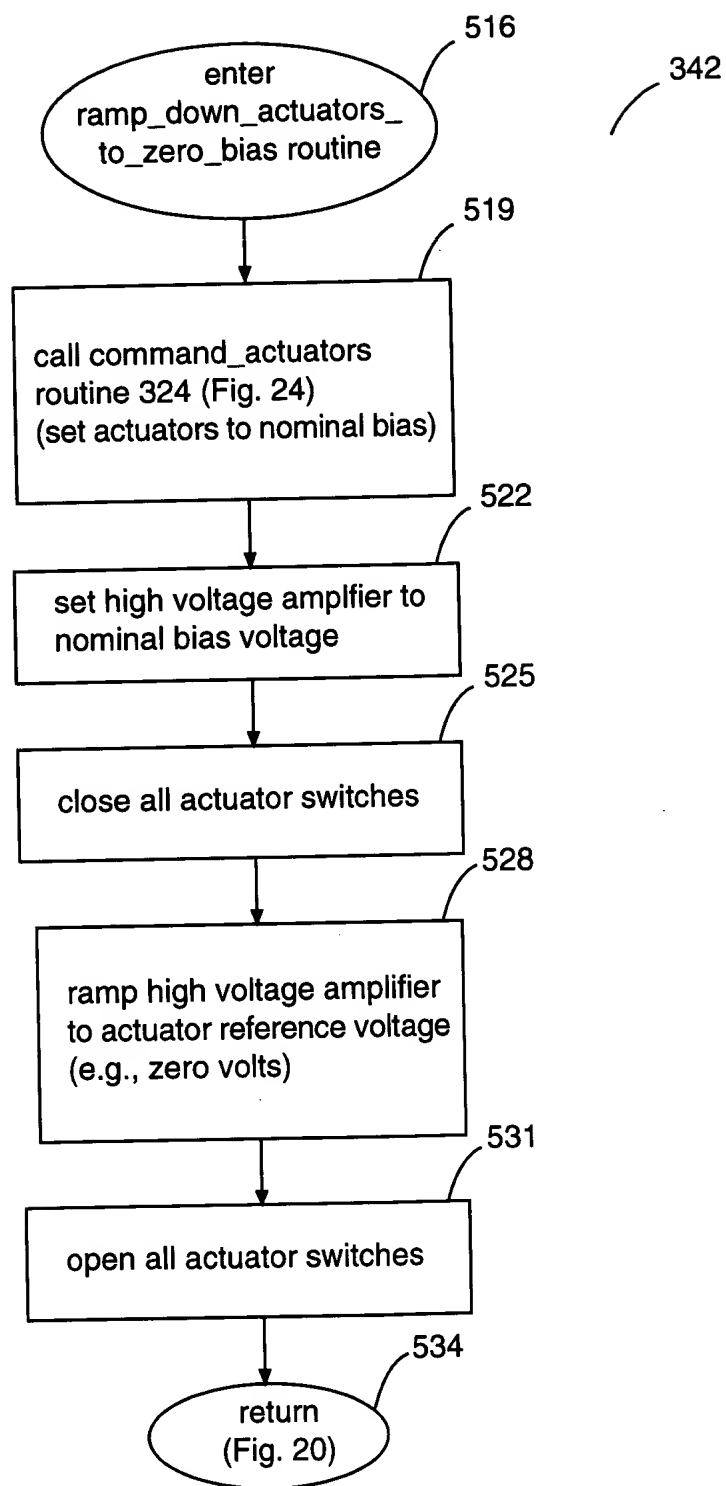


Fig. 29

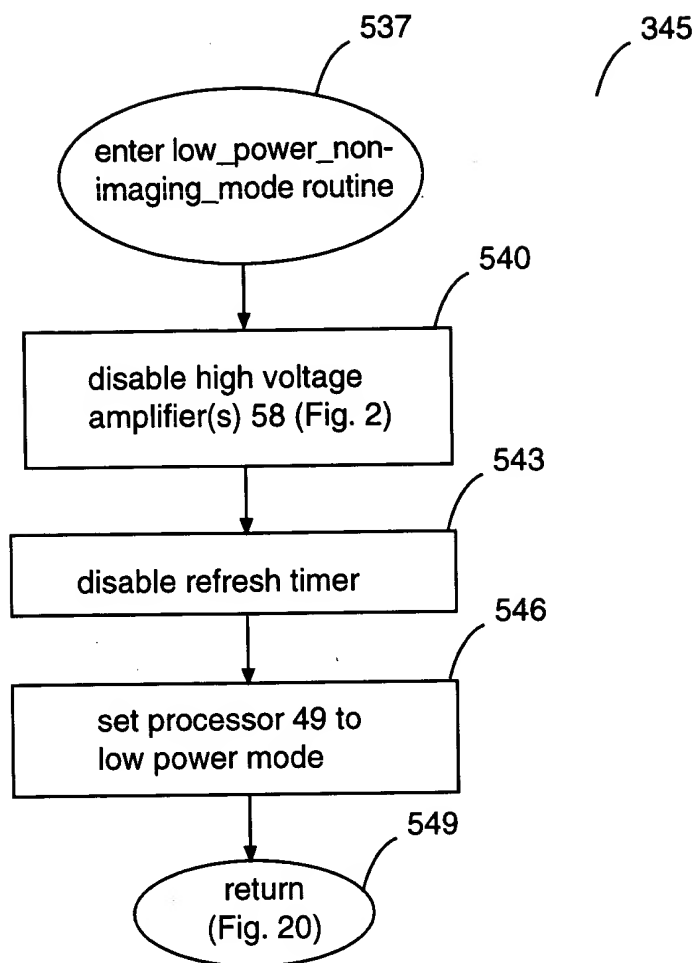


Fig. 30

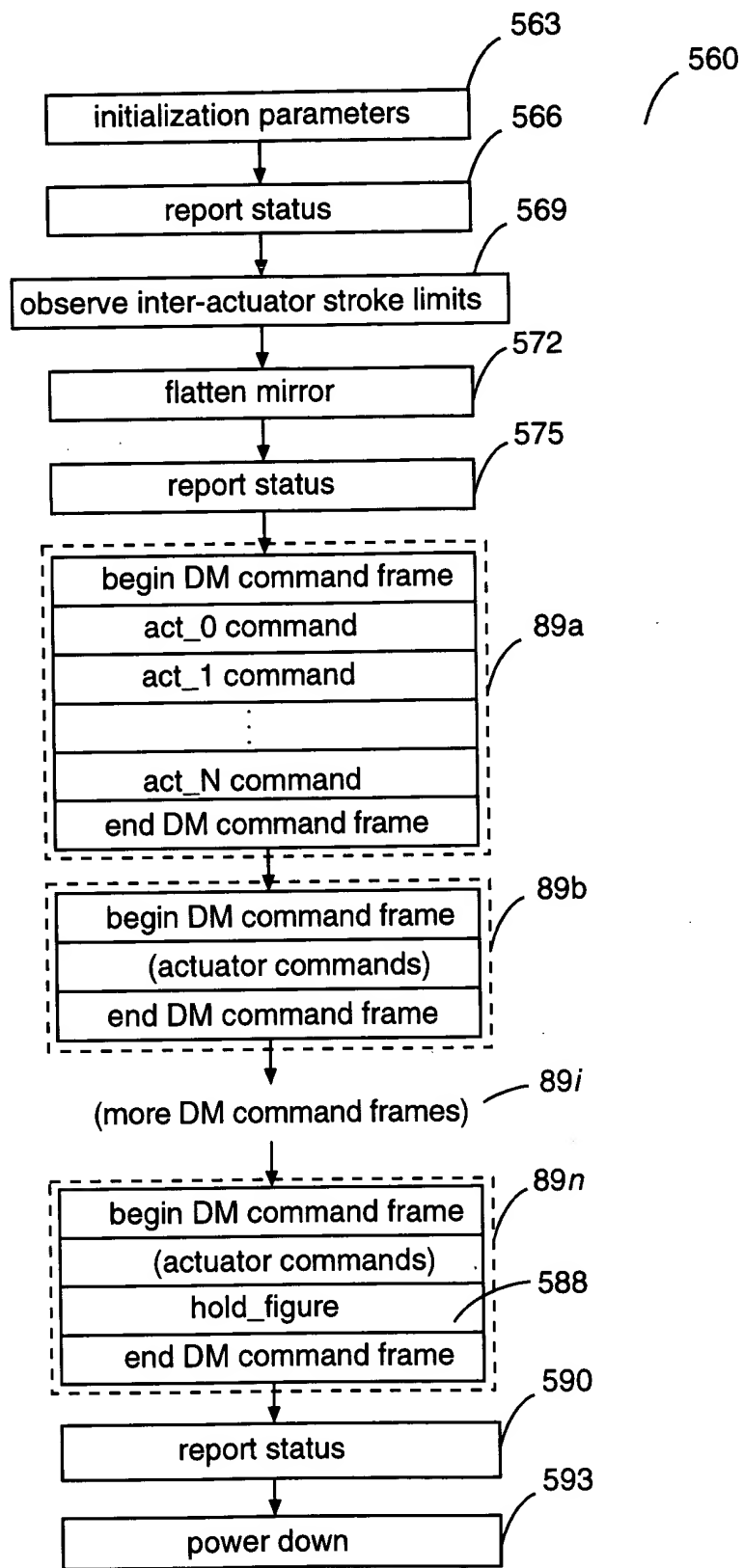
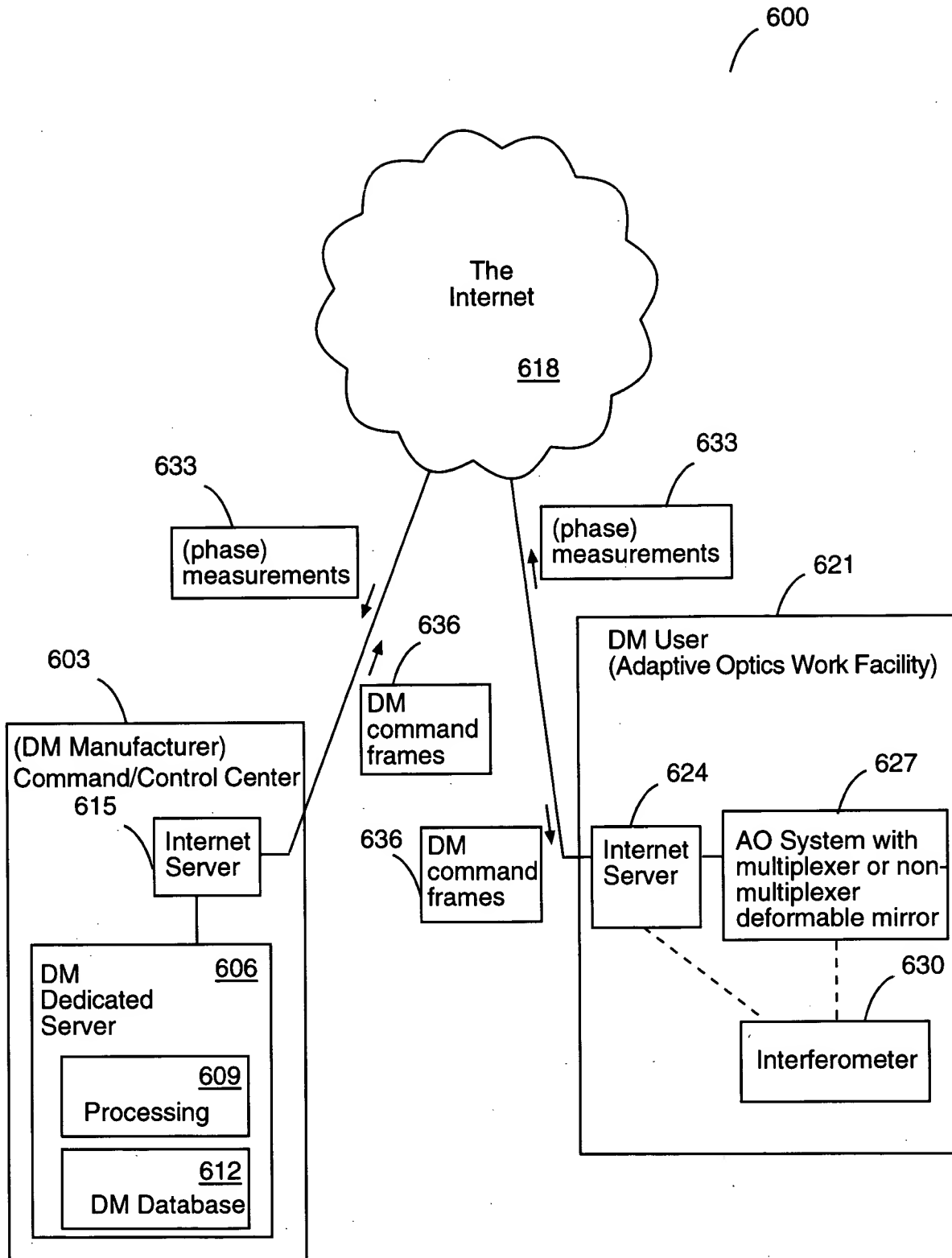


Fig. 31



space-based telescope

639

DM assy

10

642

89a

89b

Command/
Control
Center

603

Fig. 33

